AI Based Low complexity VLSI Architectures for 2D Daubechies Wavelet Filters for DSP Applications

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ABSTRACT: The field of separate rippling transforms has been attracting substantial interest partially as a result of the rippling analysis being capable of modeling an indication into a specific set of basic functions equipped with sensible spectral properties. Rippling analysis has been accustomed observe system non-linearities by creating use of its localization feature. DWT-based multi-resolution analysis results in each time and frequency localization. Separate rippling transforms square measure of interest in signal and image process as a result of their capability of signal decomposition, denoising, and event detection. This paper proposes a algebraically number primarily based multi-encoding of Daubechies-4 and -6 2-D rippling filters having error-free integer-based computation. Digital VLSI architectures using parallel channels square measure projected, physically completed and tested. The multi-encoded AI framework permits a multiplication-free and computationally correct design. It additionally guarantees a noise-free computation outturn the multi-level multi-rate 2-D filtering operation. one final reconstruction step (FRS) furnishes filtered and down-sampled image outputs in fixed-point, leading to low levels of division noise.

KEYWORDS: Final reconstruction step, DWT, AI

I. INTRODUCTION

The DWT has extensively been utilized in a large variety of applications with numerical analysis, image and video cryptography, pattern recognition, medical and telemetric imaging, etc. The DWT decomposition by mallat shows that DWT may be viewed as a multiresolution decomposition of signal. DWT implies it decomposes the signal into its parts in several frequency bands. The Inverse DWT will   reconstruct the signal from its octave band parts. Once its inclusion in JPEG 2000 compression normal, important analysis has been done to optimize the DWT implementation to cut back the procedure complexness. Among a large vary of wavelets, the Daubechies wavelets embody members starting from extremely localized to extremely sleek and might give glorious performance in compression [1] .Among the members of the family, the primary two applications. Whereas pressure medical pictures, the key here is to preserve the maximum amount crucial info as potential within the reconstructed image in order that correct identification is feasible. There are many economical implementations of ripple filters projected for applications in image process and Daubechies 6-tap area unit fashionable selections in medical imaging. The employment of standard fixed-point binary illustration for implementing separate riffle coefficients introduces round-off or approximation errors at the terribly starting of the method [8]. The error is as a result of the dearth of tangible illustration of the irrational numbers that kind the constant basis.

These errors tend to expand because the calculations progress through the design, degrading the standard of image reconstruction. A lossless mapping technique, referred to as pure mathematics whole number quantisation, may be wont to minimize the approximation error and expeditiously calculate the DAUB4 and DAUB6 coefficients.

The AI theme is split into two half, the first stage is predicated on factorisation and decomposition of remodel matrices exploiting the radially symmetrical structure. Once the decomposition, we tend to map the irrational remodel basis coefficients mistreatment four-dimensional pure mathematics integers that lead to precise illustration and less complicated implementation [7].

II. RELATED WORK

In the AI illustration, irrational numbers concerned within the DWT method ar encoded into integers associated to a given AI basis. The computing design is replaced with a parallel channel model [2].once computation, ensuing encoded numbers ar mapped into fixed-point illustration within the final reconstruction step (FRS). The FRS is that the solely doable supply of machine error during agiven AI-based framework.

AI cryptography will address the machine noise injection in ripple analysis systems [6]. A major advantage of the AI cryptography is its capability of mapping the required irrational ripple coefficients into vectors or arrays of integers. Therefore, wavelet decomposition is often performed while not errors during a vectorial framework consisting completely of number operations. Thus, the irrational coefficients of the Daubechies filters are often diagrammatical into integers, in step with a specific AI basis.

III. DAUBECHIES WAVELETS

This section provides a introduction to Daubechies wavelets. These wavelets include members starting from extremely localized to extremely sleek Daubechies-2 to Daubechies-20 and conjointly provide glorious performance in compression. The Daubechies moving ridge coefficients square measure supported computing moving ridge coefficients.

1. The conservation of space underneath a finite length

2. The accuracy conditions

3. The proper reconstruction conditions

The Daub-4 wavelets square measure typically used in applications wherever the signals square measure sleek and slowly variable, the Daub-6 wavelets square measure used for signals bearing abrupt changes, spikes, and having high unwanted noise levels. Daubechies-4 and -6 faucet filter coefficients square measure irrational varietys and can't be delineated specifically in commonplace finite preciseness number systems like the two's complement fixed-point format,the fixed-point representations incur errors once used in arithmetic processors. These errors, as a result of quantisation, overflow, and underflow, propagate through the complete method of moving ridge decomposition. The results of the moving ridge analysis possess a reduced ratio. Typical 2-D Daubechies-4 and -6 filter banks use 1-D filters as their building block. The 1-D Daubechies-4 filters measure repeatedly applied to row and column wise operations to yield 2-D filtering.
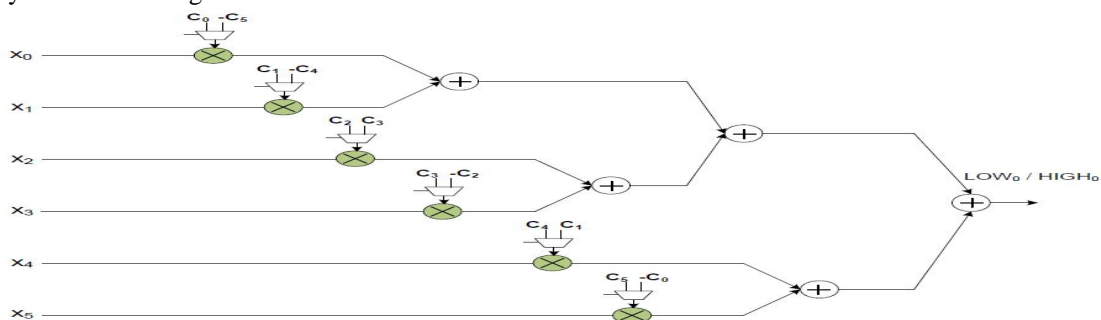

Figure 1. FP-based DAUB6 filter architecture

A.The Problem of Fixed-Point Errors

Filter banks associated to Daubechies wavelets have irrational coefficients whose illustration in fixed-point needs truncation or estimation [2, 6, and 16]. Such approximations introduce illustration errors that propagate through a given filter bank. Moreover, the longer the desired filter bank provides larger process error could become. This method affects a lower obtained ratio of the ensuing knowledge.

B .AI Based 4-Tap and 6-Tap 2-D Daubechies Wavelet Filter Banks

In propose a replacement multi-encoding technique that achieves precise computation of multi-level 2-D Daubechies rippling transforms mistreatment algebraically number secret writing. Compared to existing AI styles in literature [1, 3, 6], the planned style will cipher rippling image approximations entirely over number fields and with one FRS in a very strictly AI based mostly 2-D design. The planning avoids the requirement of intermediate reconstruction steps.

Moreover, the planned design is sought-after to be multiplier-free. Such style facilitates accuracy, speed, and comparatively smaller space on chip further as value of style. The new style is multi-encoded and multi-rate, in operation over AI with no intermediate reconstruction steps. During this framework, error-free computations are performed till the ultimate FRS. Our design emphasizes on quality of output image and speed by commerce complexness and power consumption for accuracy.
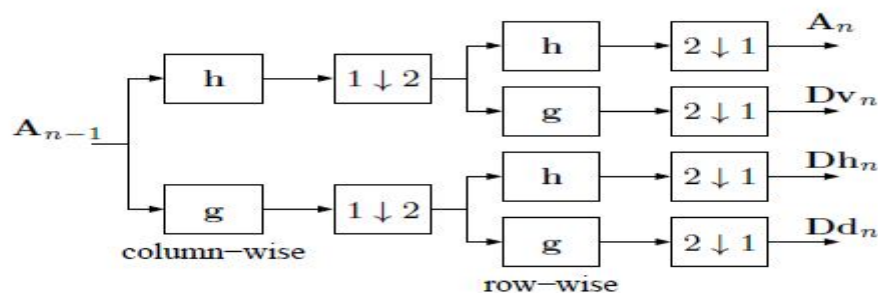

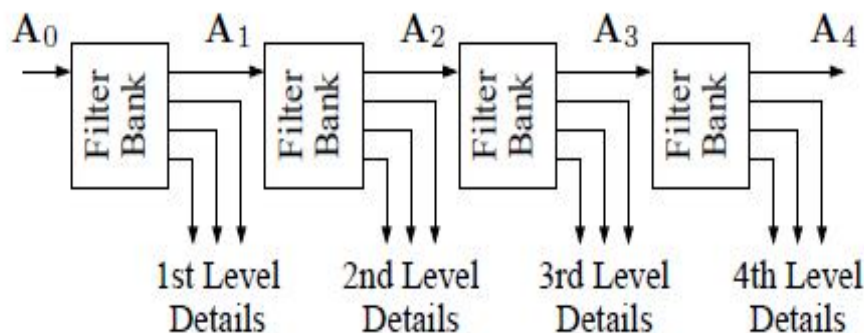Figure 2.Diagram of a single application of the 2-D wavelet filter bank.

Figure 3. Recursive application of the 2-D wavelet filter bank

Proposed AI encoding will address the process noise injection in rippling analysis systems [6]. A big advantage of the AI secret writing is its capability of mapping the desired irrational rippling coefficients into vectors or arrays of integers. Therefore, rippling decomposition is performed while not errors in a very vectorial framework

consisting solely of number operations. Thus, the irrational coefficients of the Daubechies filters are described into integers, consistent with a particular AI basis [3, 6].
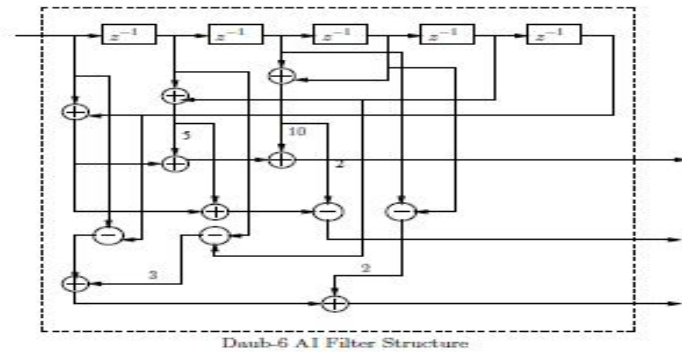

Figure 4. Daub-6 AI Filter Structure

IV. EXPANSION FACTOR METHOD

Expansion factors are scaling constants sometimes used within the style of approximate transforms. Survey the subject during this context. Recently this system was extended and custom-made to the look of ultimate reconstruction blocks associated with AI based mostly architectures .The enlargement issue methodology is anticipated to supply higher results for larger basis. Indeed, the Daub-4 design couldn't like the enlargement methodology since its basis contains just one non-unity element:ζ .

However, as a result of the AI basis associated with the Daub-6 theme has 3 non-unity components ζ_1, ζ_2, $\zeta_1\zeta_2$, the enlargement issue methodology could lead on to helpful architectures within the FRS following procedure search algorithms for appropriate number mixtures. Within the next section we offer activity results regarding the enlargement issue methodology.

V. FPGA IMPLEMENTATION AND RESULTS

The architectures for Daub-4 and -6 filter banks were implemented on Xilinx Virtex xc6vcx240t-1ff1156 device using the ML605 evaluation board. The designs were tested with six different standard images obtained from . Gray 512×512 images Woman, Cameraman, and Reflection to the Daub-4 filter banks whereas Mandrill, Lena, and CT head were submitted to the Daub-6 filter banks. Hardware results were verified with Matlab, hardware results from the Xilinx FPGA for the Daub-4 and -6 filter banks. Table 1 shows a performance comparison among proposed Daub-4 and -6 architectures for single level decomposition of 8-bit Lena image. For comparison, we devised a version of the proposed system that operates over fixed-point arithmetic instead of AI-based arithmetic. For such, we employed 8 bits for word size with 6 fractional bits. In this case, the required filter banks were implemented by quantizing the exact filter coefficients into the fixed-point representation. Notice that the fixed-point scheme incurs coupled quantization noise, whereas the AI-based architecture is immune to this source of contamination.

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The AT product may be a customary performance metric in digital hardware de- signs. It refers to chip-area and speed of the look. Lower AT values indicate a better speed of operation. In an FPGA, the realm is provided by the amount of slice LUTs used for logic given by the FPGA style tool referred to as XFLOW and therefore the time is just the crucial path delay. Amount $AT2$ is helpful, once clock speed is that the driving issue of style improvement, for high-throughput realizations.
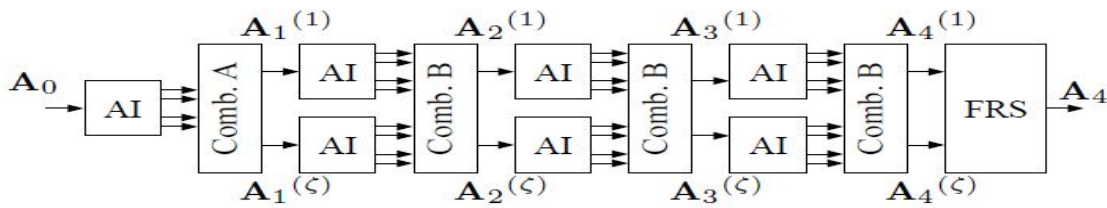

Figure 5 Multi-level AI filter bank with final reconstruction step (FRS)
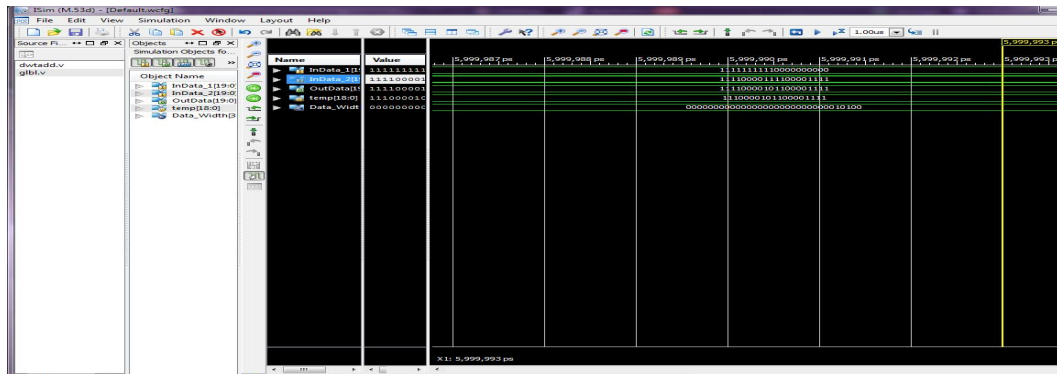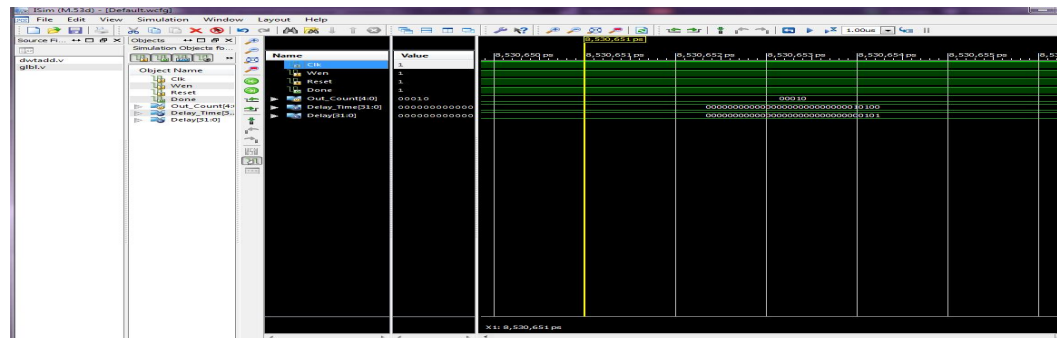

Figure 6 AI Result
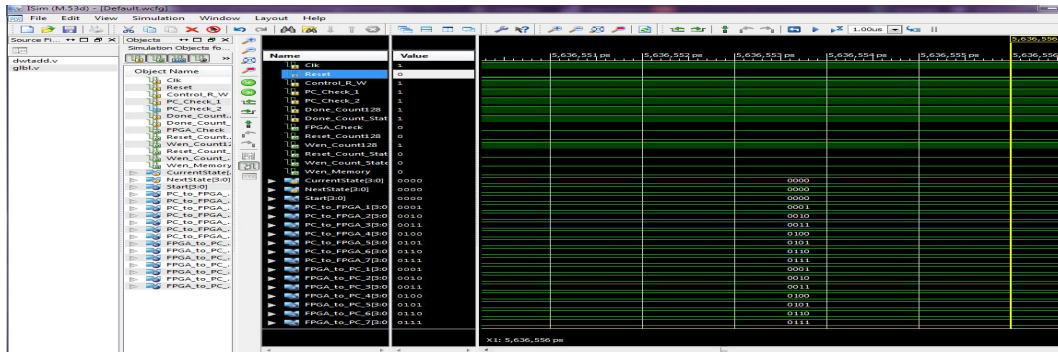

Figure 7 AI Data selection path

Figure 8 Proposed AI Encoding with encoding algorithms - 4 Tap

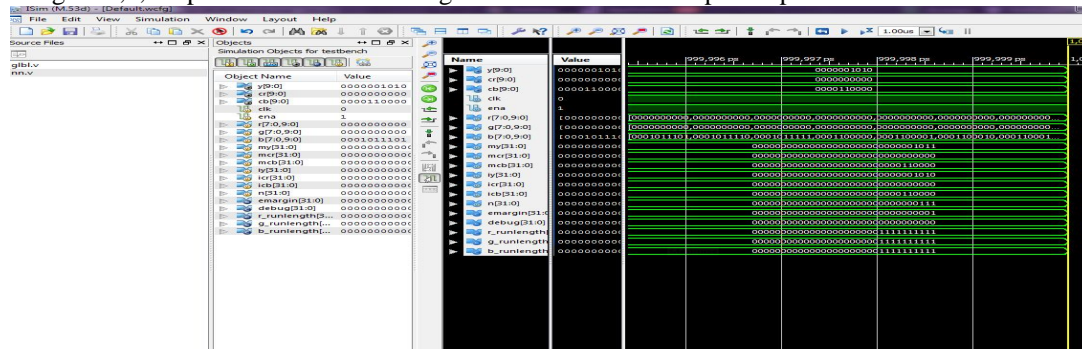In figure 6,7,8 represents the AI encoding scheme with desired input output.

Figure 9 Proposed AI Encoding with encoding algorithms – 6 Tap

ALGORITHM	AREA IN TERMS OF GATE COUNT	POWER IN mW	DELAY IN ns
AI without encoding algorithm 4 Tap	12,944	8784	21.9
AI without encoding algorithm 6 Tap	3000	10101	4.43
AI with encoding algorithm 6 Tap	14,735	18,720	38.45
AI with encoding algorithm 4 Tap	4276	13279	11.27

Table 1 .Comparison table 4 Tap and 6 Tap Filter

VI. RESULTS AND DISCUSSION

Xilinx power analyzer was used to research the facility consumption on Xilinx FPGA Virtex-6 device. The quiescent power dissipation may be a combined result of standby and discharge power dissipations. At forty nm method technology static power dominates dynamic power. Dynamic power represents the unsteady power because the style runs and is that the add of short-circuit and electrical phenomenon power dissipations. The figures 6, 7, 8,9,10 represent the performance analysis of 4 Tap and 6 Tap filter .The proposed AI based multi encoded algorithm having reduced amount of gate count and power consumption.

VII. CONCLUSIONS

We planned associate degree optimized multi-rate 1-D/2-D Daub-4 and Daub-6 filter bank architectures that area unit strictly AI-based, and multi-encoded. In addition, the introduced styles area unit capable of furnishing willy-nilly high numerical accuracy mistreatment error-free whole number arithmetic. In fact, the planned architectures preserve all options of our earlier architectures like (i) Error-free computation with reduced delay, (ii) outlined over integers with reduced power, and (iii) freed from multiplications with scale back part quality. It additionally reduces hardware quality (number of adders) resulting in sizeable reduction in price for the hardware realization of multi-level 2-D DWTs of Daubechies 4-tap and 6-tap filter banks. The FRS is that the only supply of process error. By using AI coding, ensuing ripple rotten pictures had SNR and PSNR figures improved by close to 30–35% compared to a counter- half fixed-point system with 8-bit word length and six fragmental bits.

REFERENCES

[1] K. Wahid, V. Dimitrov, and G. Jullien. VLSI architectures of Daubechie wavelets for algebraic integers. Journal of Circuits, Systems, and Computers,13(6):1251–1270, 2004.

[2] K. A. Wahid, V. S. Dimitrov, G. A. Jullien, and W. Badawy. An algebraic integer based   encoding scheme for implementing Daubechies discrete wavelet transforms. In Asilomar Conf. Signals, Syst. Comp., volume 1, pages 967–971,2002.

[3] K. A. Wahid, V. S. Dimitrov, G. A. Jullien, and W. Badawy. An analysis of Daubechies discrete wavelet transform based on algebraic integer encoding scheme. In Proc. Third Int. Workshop Digital and Computational Video DCV 2002, pages 27–34, 2002.

[4] Guiwei Xing, Jin Li, Shipeng Li, and Ya-Qin Zhang. Arbitrarily shaped video object coding by wavelet. 11(10):1135–1139, 2001.

[5] Yan Wu, R. J. Veillette, D. H. Mugler, and T. T. Hartley. Stability analysis of wavelet-based   controller design. In Proc. American Control Conf the 2001,volume 6, pages 4826–4827,   2001.

[6] K. A. Wahid, V. S. Dimitrov, and G. A. Jullien. Error-free arithmetic for discrete wavelet transforms using algebraic integers. In Proc. 16th IEEE Symp. Computer Arithmetic, pages 238–244, 2003.

[7] S.-C. B. Lo, Huai Li, and M. T. Freedman. Optimization of wavelet decomposition for image compression and feature preservation. 22(9):1141–1151, 2003.

[8] M.Martone. Multiresolution sequence detection in rapidly fading channels based on focused wavelet decompositions. 49(8):1388–1401, 2001.

[9] P. P. Vaidyanathan. Multirate Systems and Filter Banks. PTR Prentice Hall Englewoodcliffs, New Jersey 07632, 1992.

[10] B.K. Mohanty and P.K. Meher. Merged-cascaded systolic array for vlsi implementation of discrete wavelet transform. In Circuits and Systems, 2006.APCCAS 2006. IEEE Asia Pacific Conference on, pages 462–465, 2006.